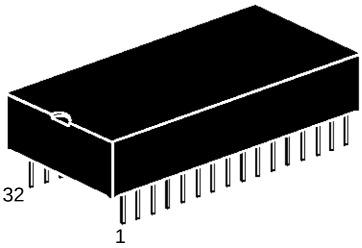
SGS-THOMSON
MICROELECTRONICS

M48Z128
M48Z128Y

CMOS 128K x 8 ZEROPOWER SRAM

- INTEGRATED LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT and BATTERY
- CONVENTIONAL SRAM OPERATION; UNLIMITED WRITE CYCLES
- 10 YEARS of DATA RETENTION in the ABSENCE of POWER
- PIN and FUNCTION COMPATIBLE with JEDEC STANDARD 128K x 8 SRAMs
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- CHOICE of TWO WRITE PROTECT VOLTAGES:
  - M48Z128: $4.5V \leq V_{PFD} \leq 4.75V$
  - M48Z128Y: $4.2V \leq V_{PFD} \leq 4.50V$
- BATTERY INTERNALLY ISOLATED UNTIL POWER IS APPLIED



PMDIP32 (PM)
Module

DESCRIPTION

The M48Z128/128Y 128K x 8 ZEROPOWER® RAM is a non-volatile 1,048,576 bit Static RAM organized as 131,072 words by 8 bits. The device combines an internal lithium battery and a full CMOS SRAM in a plastic 32 pin DIP Module.

Table 1. Signal Names

A0 - A16	Address Inputs
DQ0 - DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

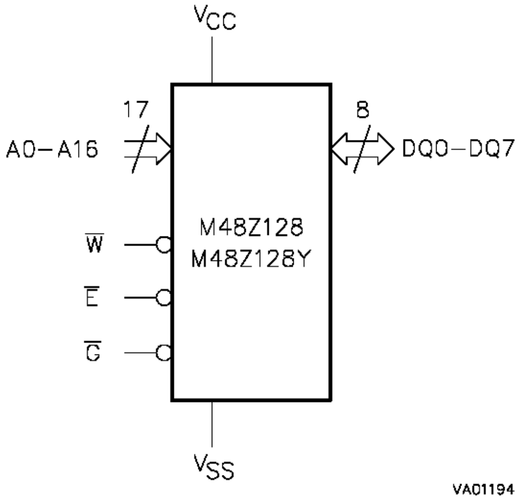


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature (V_{CC} Off)	–40 to 70	°C
T_{BIAS}	Temperature Under Bias	–10 to 70	°C
T_{SLD}	Lead Soldering Temperature for 10 seconds	260	°C
V_{IO}	Input or Output Voltages	–0.3 to 7	V
V_{CC}	Supply Voltage	–0.3 to 7	V

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

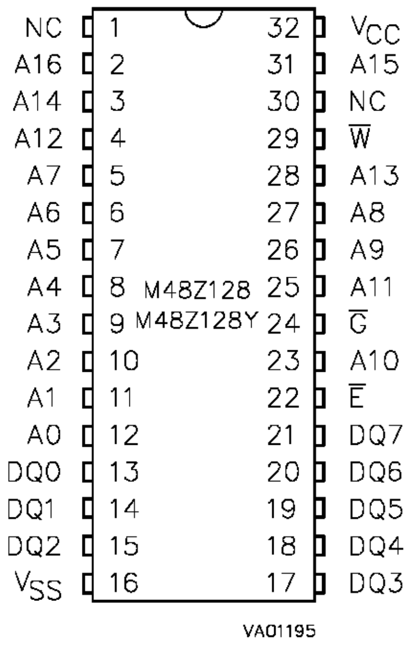
***CAUTION:** Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

Table 3. Operating Modes

Mode	V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	4.75V to 5.5V or 4.5V to 5.5V	V_{IH}	X	X	High Z	Standby
Write		V_{IL}	X	V_{IL}	D_{IN}	Active
Read		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
Read		V_{IL}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min)	X	X	X	High Z	CMOS Standby
Deselect	$\leq V_{SO}$	X	X	X	High Z	Battery Back-up Mode

Note: X = V_{IH} or V_{IL}

Figure 2. DIP Pin Connections



DESCRIPTION (cont'd)

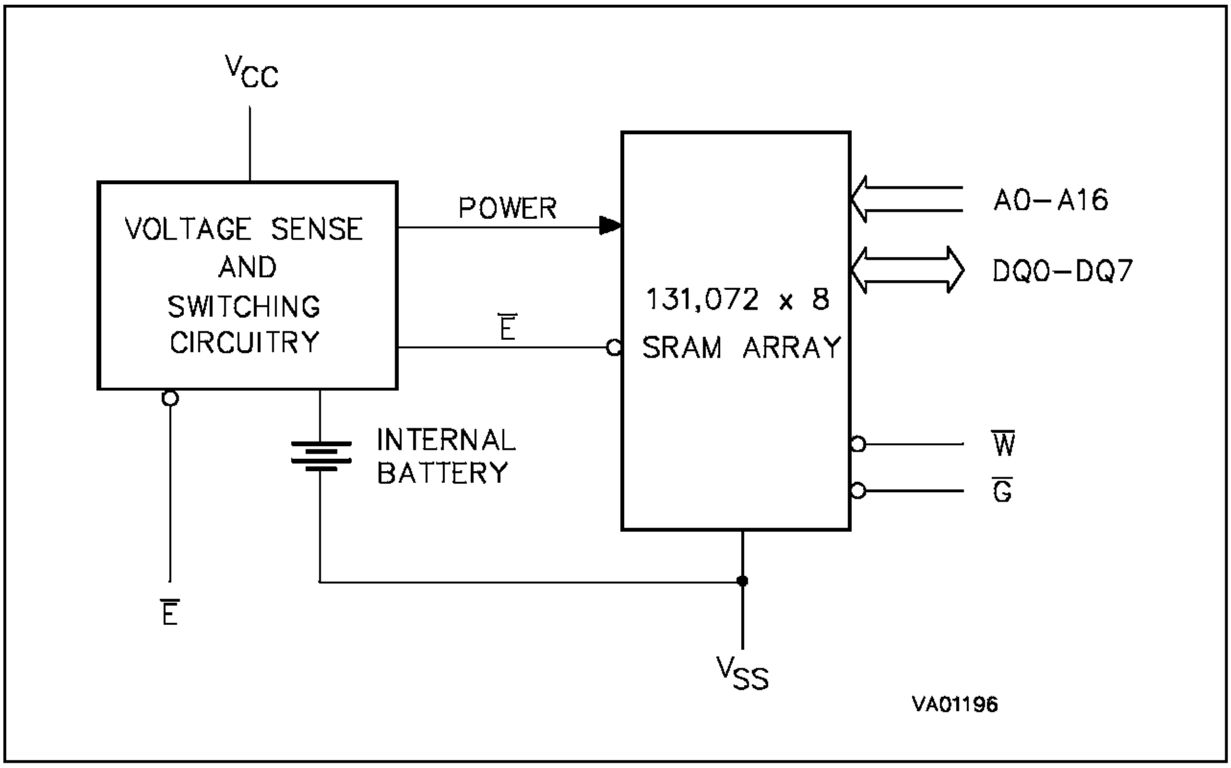
The ZEROPOWER RAM directly replaces industry standard SRAMs. It also fits into many EPROM and EEPROM sockets, providing the nonvolatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

The M48Z128/128Y has its own Power-fail Detect Circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operations brought on by low V_{CC}. As V_{CC} falls below approximately 3V, the control circuitry connects the battery which sustains data until valid power returns.

READ MODE

The M48Z128/128Y is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low. The device architecture allows ripple-through access of data from eight of 1,048,576 locations in the static storage array. Thus, the unique address specified by the 17 Address Inputs defines which

Figure 3. Block Diagram



one of the 131,072 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} (Address Access Time) after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ (Output Enable) access times are also satisfied. If the $\overline{E}$ and $\overline{G}$ access times are not met, valid data will be available after the later of Chip Enable Access Time (t_{ELQV}) or Output Enable Access Time (t_{GLQV}).

The state of the eight three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while $\overline{E}$ and $\overline{G}$ remain low, output data will remain valid for t_{AXQX} (Output Data Hold Time) but will go indeterminate until the next Address Access.

WRITE MODE

The M48Z128/128Y is in the Write Mode whenever $\overline{W}$ and $\overline{E}$ are active. The start of a write is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit

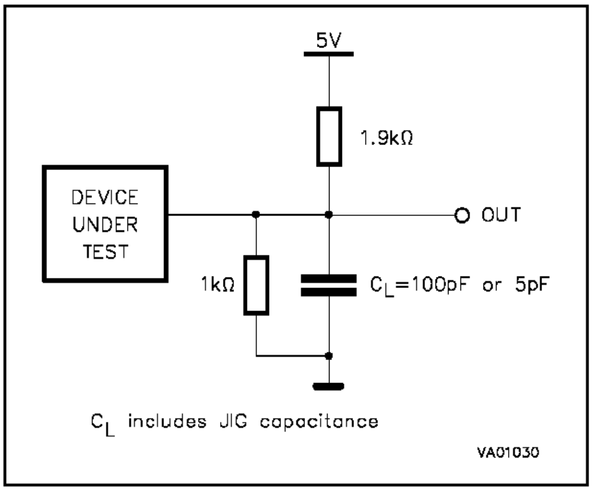


Table 4. Capacitance [1, 2] (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		10	pF
C_{IO} (3)	Input / Output Capacitance	V_{OUT} = 0V		10	pF

Notes: 1. Effective capacitance measured with power supply at 5V.
2. Sampled only, not 100% tested.
3. Outputs deselected

Table 5. DC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI} (1)	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±1	µA
I_{LO} (1)	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±1	µA
I_{CC}	Supply Current	$\overline{E}$ = V_{IL}, Outputs open		105	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		7	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ ≥ V_{CC} – 0.2V		4	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	2.4		V

Note: 1. Outputs deselected.

Table 6. Power Down/Up Trip Points DC Characteristics (1) (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{PFD}	Power-fail Deselect Voltage (M48Z128)	4.5	4.6	4.75	V
V_{PFD}	Power-fail Deselect Voltage (M48Z128Y)	4.2	4.3	4.5	V
V_{SO}	Battery Back-up Switchover Voltage		3		V
t_{DR}(2)	Data Retention Time	10			YEARS

Notes: 1. All voltages referenced to V_{SS}.
2. @ 25°C

Table 7. Power Down/Up Mode AC Characteristics (T_A = 0 to 70°C)

Symbol	Parameter	Min	Max	Unit
t_F (1)	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		µs
t_{FB} (2)	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10		µs
t_{WP}	Write Protect Time from $V_{CC} = V_{PFD}$	40	150	µs
t_R	V_{SO} to V_{PFD} (max) V_{CC} Rise Time	0		µs
t_{ER}	$\overline{E}$ Recovery Time	40	120	ms

Notes: 1. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passes V_{PFD} (min).

2. V_{PFD} (min) to V_{SO} fall time of less than t_{FB} may cause corruption of RAM data.

Figure 5. Power Down/Up Mode AC Waveforms

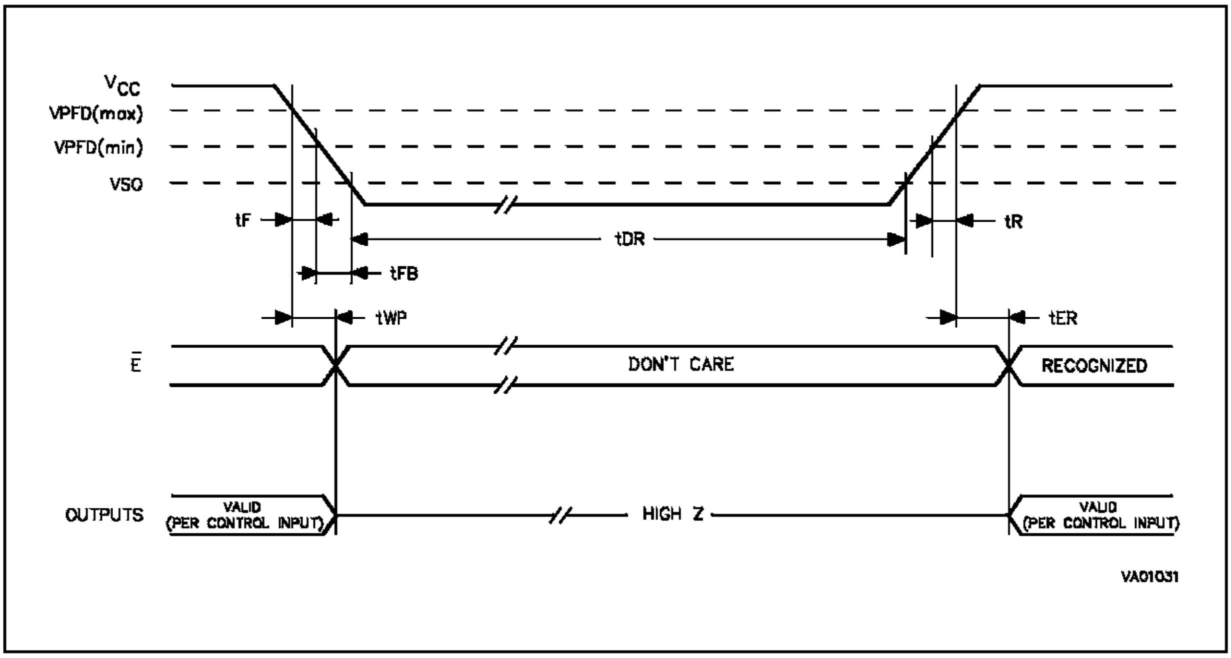
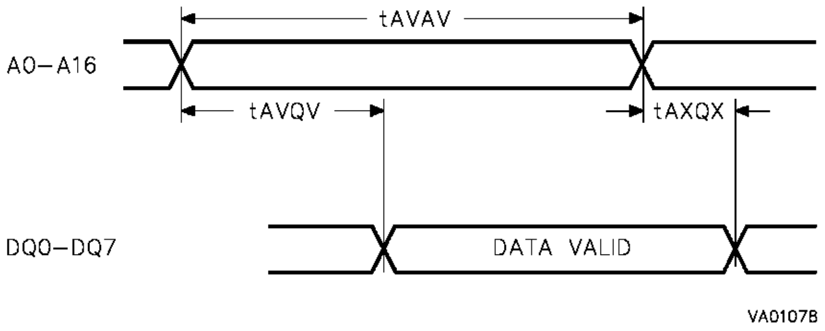


Table 8. Read Mode AC Characteristics (T$_A$ = 0 to 70°C; V$_{CC}$ = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48Z128 / 128Y				Unit
		-85		-120		
		Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time	85		120		ns
t_{AVQV} (1)	Address Valid to Output Valid		85		120	ns
t_{ELQV} (1)	Chip Enable Low to Output Valid		85		120	ns
t_{GLQV} (1)	Output Enable Low to Output Valid		45		60	ns
t_{ELQX} (2)	Chip Enable Low to Output Transition	5		5		ns
t_{GLQX} (2)	Output Enable Low to Output Transition	0		0		ns
t_{EHQZ} (2)	Chip Enable High to Output Hi-Z		35		45	ns
t_{GHQZ} (2)	Output Enable High to Output Hi-Z		25		35	ns
t_{AXQX} (1)	Address Transition to Output Transition	10		10		ns

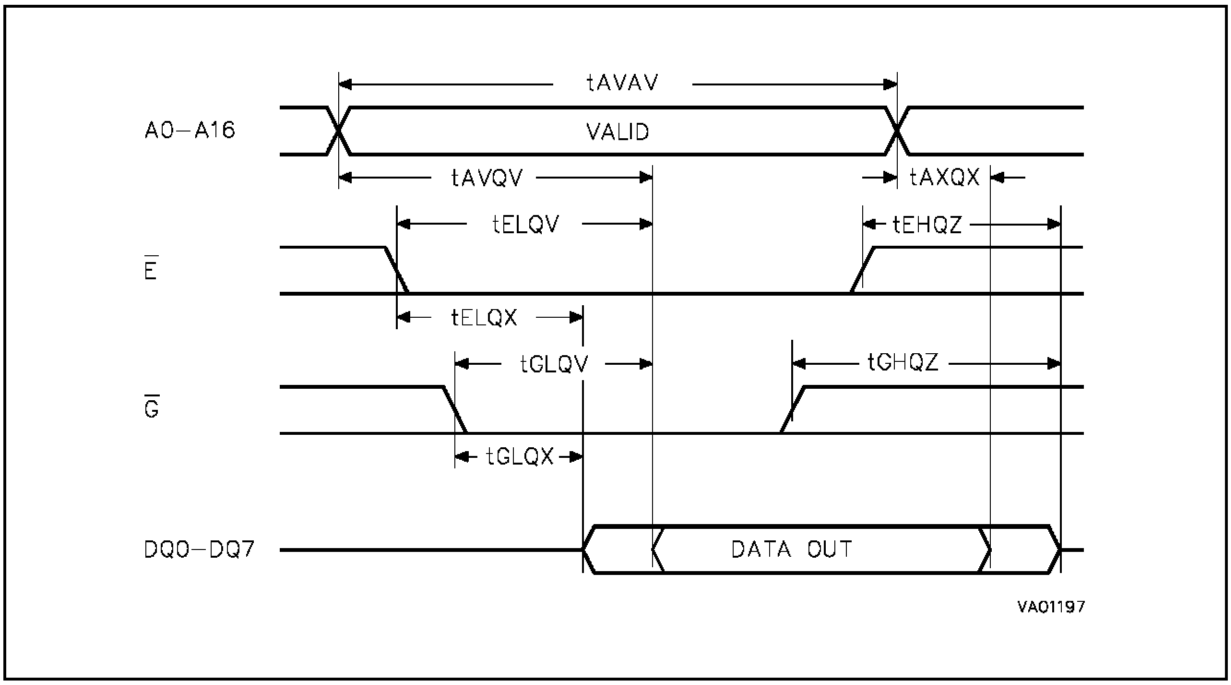
Notes: 1. C$_L$ = 100pF (see Figure 4).
2. C$_L$ = 5pF (see Figure 4)

Figure 6. Address Controlled, Read Mode AC Waveforms



Note: $\overline{E}$ = Low, $\overline{G}$ = Low, $\overline{W}$ = High.

Figure 7. Chip Enable or Output Enable Controlled, Read Mode AC Waveforms



Note: $\overline{W}$ = High.

WRITE MODE (cont'd)

The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for minimum of t_{EHAX} from $\overline{E}$ or t_{WHAX} from $\overline{W}$ prior to the initiation of another read or write cycle. Data-in must be valid t_{DVWH} prior to the end of write and remain valid for t_{WHDX} or t_{EHDX} afterward. $\overline{G}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$, a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

DATA RETENTION MODE

With valid V_{CC} applied, the M48Z128/128Y operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself t_{WP} after V_{CC} falls below V_{PFD}. All outputs become high impedance, and all inputs are treated as "don't care."

If power fail detection occurs during a valid access, the memory cycle continues to completion. If the memory cycle fails to terminate within the time t_{WP}, write protection takes place. When Vcc drops below V_{SO}, the control circuit switches power to the internal energy source which preserves data.

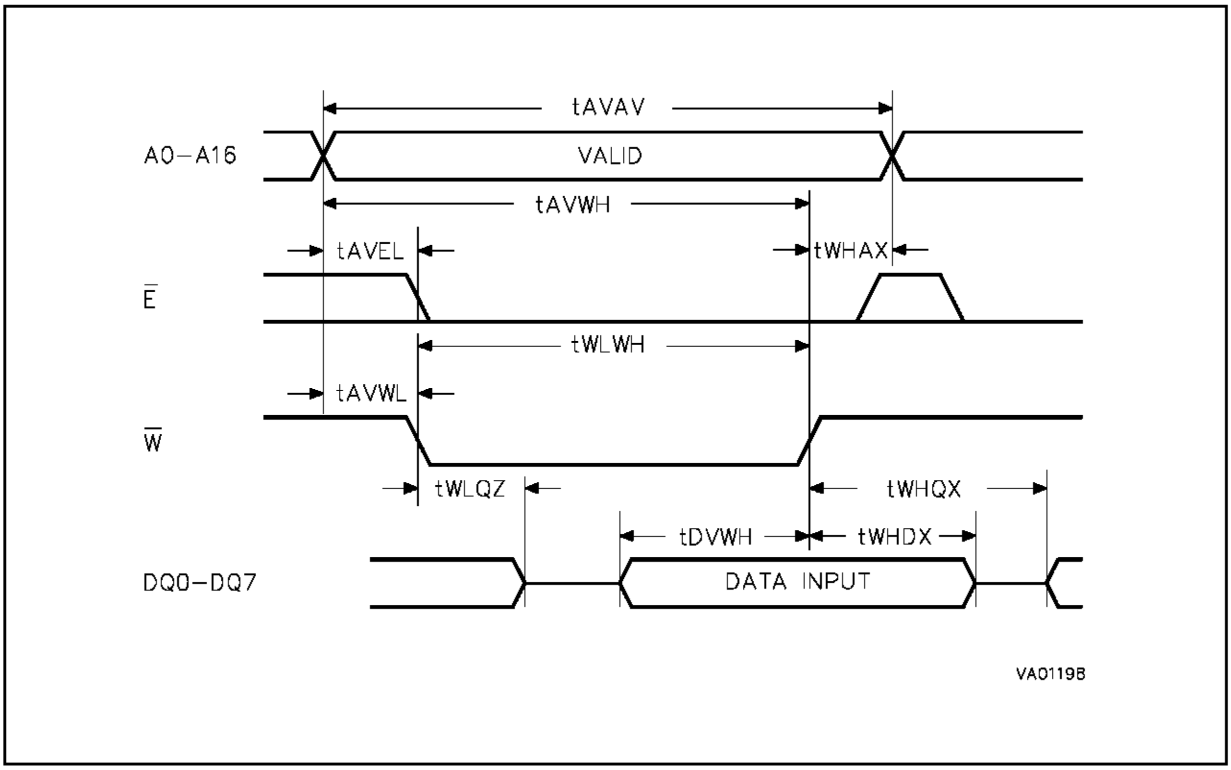
The internal coin cell will maintain data in the M48Z128/128Y after the initial application of V_{CC} for an accumulated period of at least 10 years when V_{CC} is less than V_{SO}. As system power returns and Vcc rises above V_{SO}, the battery is disconnected, and the power supply is switched to external Vcc. Write protection continues for t_{ER} after V_{CC} reaches V_{PFD} to allow for processor stabilization. After t_{ER}, normal RAM operation can resume.

Table 9. Write Mode AC Characteristics (T_A = 0 to 70°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48Z128 / 128Y				Unit
		-85		-120		
		Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time	85		120		ns
t_{AVWL}	Address Valid to Write Enable Low	0		0		ns
t_{AVEL}	Address Valid to Chip Enable Low	0		0		ns
t_{WLWH}	Write Enable Pulse Width	65		85		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	75		100		ns
t_{WHAX}	Write Enable High to Address Transition	5		5		ns
t_{EHAX}	Chip Enable High to Address Transition	15		15		ns
t_{DVWH}	Input Valid to Write Enable High	35		45		ns
t_{DVEH}	Input Valid to Chip Enable High	35		45		ns
t_{WHDX}	Write Enable High to Input Transition	0		0		ns
t_{EHDX}	Chip Enable High to Input Transition	10		10		ns
t_{WLQZ} (1,2)	Write Enable Low to Output Hi-Z		30		40	ns
t_{AVWH}	Address Valid to Write Enable High	75		100		ns
t_{AVEH}	Address Valid to Chip Enable High	75		100		ns
t_{WHQX} (1,2)	Write Enable High to Output Transition	0		0		ns

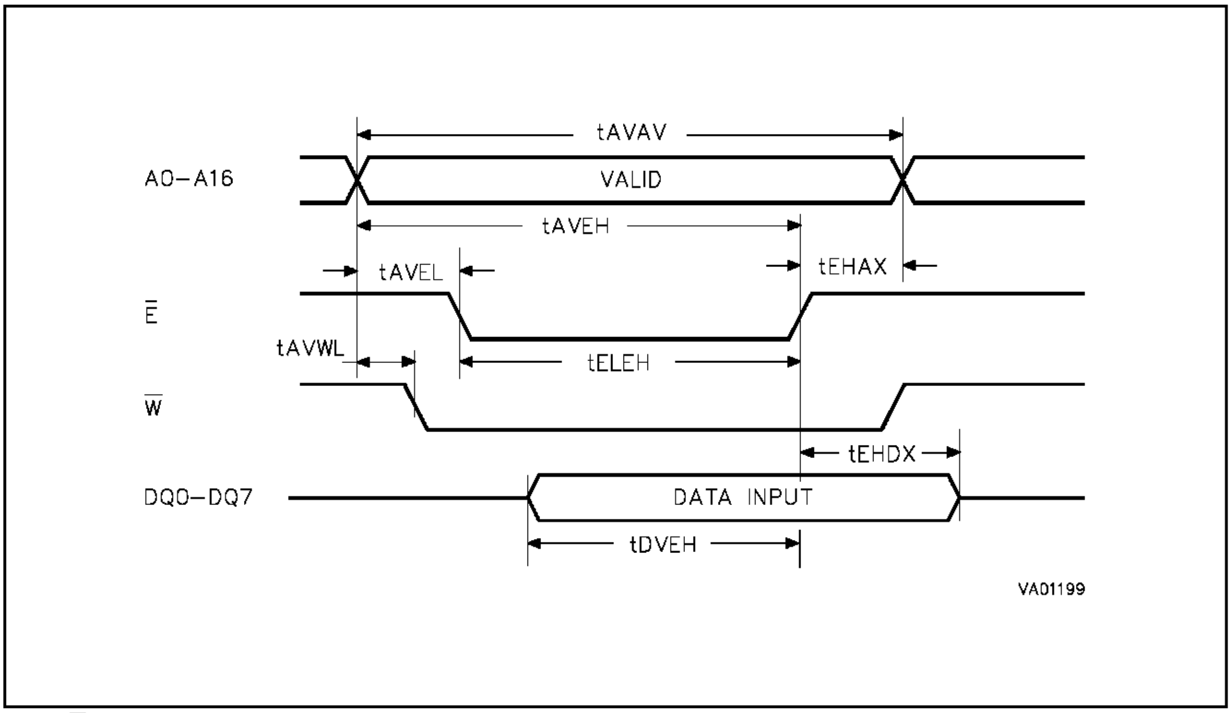
Notes: 1. C_L = 5pF (see Figure 4).
2. If $\overline{E}$ goes low simultaneously with $\overline{W}$ going low after $\overline{W}$ going low, the outputs remain in the high-impedance state.

Figure 8. Write Enable Controlled, Write AC Waveforms



Note: $\overline{G}$ = High.

Figure 9. Chip Enable Controlled, Write AC Waveforms



Note: $\overline{G}$ = High.

ORDERING INFORMATION SCHEME

Example: M48Z128Y -85 PM 1

Supply Voltage and Write Protect Voltage		Speed		Package		Temp. Range	
128	V_{CC} = 4.75V to 5.5V V_{PFD} = 4.5V to 4.75V	-85	85ns	PM	PMDIP32	1	0 to 70°C
128Y	V_{CC} = 4.5V to 5.5V V_{PFD} = 4.2V to 4.5V	-120	120ns				

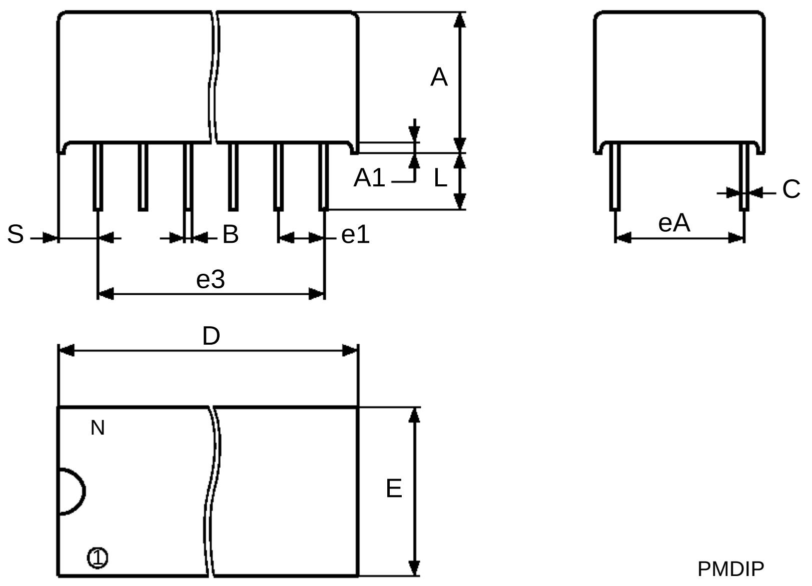
For a list of available options (Package and Speed) refer to the current Memory Shortform catalogue.

For further information or any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

PMDIP32 - 32 pin Plastic DIP Module

Symb	**mm**			**inches**		
	Typ	**Min**	**Max**	**Typ**	**Min**	**Max**
A		9.27	9.52		0.365	0.375
A1		0.38	–		0.015	–
B		0.43	0.59		0.017	0.023
C		0.20	0.33		0.008	0.013
D		42.42	43.18		1.670	1.700
E		18.03	18.80		0.710	0.740
e1		2.29	2.79		0.090	0.110
e3		34.29	41.91		1.350	1.650
eA		14.99	16.00		0.590	0.630
L		3.05	3.81		0.120	0.150
S		1.91	2.79		0.075	0.110
N	32			32		

PMDIP32



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